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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,372	04/09/2004	Anders Landin	5181-94901	1210
58467	7590	12/26/2007		
MHKKG/SUN P.O. BOX 398 AUSTIN, TX 78767			EXAMINER ELAND, SHAWN	
			ART UNIT 2188	PAPER NUMBER
			MAIL DATE 12/26/2007	DELIVERY MODE PAPER

Please find below, and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/821,372	Applicant(s) LANDIN ET AL.	
	Examiner Shawn Eland	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to the Applicant's response filed on 10/10/07.

Status of Claims

Claims 1 – 32 are pending in the Application.

Claims 1, 7 – 8, 13, 18 – 21, & 24 have been amended.

Claims 1 – 32 are rejected.

Response to Arguments

Applicant's arguments filed 10/10/07 have been fully considered but they are not persuasive.

The Examiner fails to see how the kind of memory used matters in this regard. If the cache memory of Liencres performs the same functions as the system memory in Applicant's invention, would that not also mean that the Liencres memory could also be considered system memory? Due to the memory's functions, there is no appreciable difference between the two memories and therefore the Examiner considers them to be one and the same for this application.

Memory simply stores data. In order to get the data there must be some kind of controller or manager that knows what to get and send the data out. The data is sent from the memory to the active device via this controller. This is how the Examiner interpreted the claim language for system memory sending data or a report.

Finally, Applicant claims Chandrasekaran does not disclose sending the data whether or not it is valid. Examiner respectfully disagrees. The whole point of optimistic reads is to start sending data before validation. Whether or not the validity checking may be performed before the downloading of data is complete is irrelevant. The word "optimistic" is used to show that data is sent without regard to validity. If the system sends a data packet that is subsequently found invalid, then a new updated packet will be sent as opposed to just the validation packet that would be sent if the data packet were valid.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Liencre* (5,434,993) in view of *Chandrasekaran* (US 6,970,872) and *Roy* (US 6,065,092).

In regards to claim 1, Liencre teaches a node including an active device (*see element 21*), a system memory (*see element 37*), and an interface interconnected by an address network and a data network (*see element 31*); an additional node coupled to send a coherency message to the interface in the node via an inter-node network, wherein the coherency message requests an access right to a coherency unit (*see figure 3a; see column 6, lines 11 – 15*).

In regards to claim 13, Liencres teaches a plurality of devices including a system memory (*see element 37*), an active device (*see element 21*), and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node system (*see element 31*); an address network configured to convey address packets between the plurality of devices (*see element 33*); a data network configured to convey data packets between the plurality of devices (*see element 33*).

In regards to claim 24, Liencres teaches an interface in the node receiving a coherency message requesting an access right to a coherency unit via the inter-node network from an additional interface in the additional node (*see element 33*).

For claims 1, 13, & 24, Liencres does not teach wherein in response to the coherency message, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state is not the modified state; wherein in response to the second type of packet, the system memory is configured to send a data packet corresponding to the coherency unit on the data network, regardless of whether the system memory has an ownership responsibility for the coherency unit.

However, Chandrasekaran teaches a multi-node network (*figure 1*) that employs several techniques to reduce latency. One of the methods is called an “optimistic read” (*col. 2, lines 54 – 57*) where the system sends the read data regardless of whether or not the data is valid (i.e. modified) (*col. 2, lines 60 – 62*). If a request made, its validity is determined. A message is sent granting or denying access to the resource based on its validity. One of the methods of determining validity is “write-time” validity checking (*col. 6, lines 25 – 36*). When another node

writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will now have to request the updated data from an additional node. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ optimistic reading of data using “write-time” validity checking so that reads could be employed when another node has exclusive access but hasn’t yet written the data.

Also in regard to claims 1, 13, & 24 Liencres does not teach wherein the node has a data network that is separate from the address network. However, it is well known in the art to have separate data and address networks, as cited in Roy (*col. 3, lines 61 – 67 through col. 4, lines 1 – 5*). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Liencres’s invention by separating the network into separate address and data networks in order to improve performance using interleaving.

For claims 2, 14, & 25, Liencres teaches the coherency message requests a read access right to the coherency unit (*see column 7, “Read Transactions”*), wherein the first type of address packet is a proxy read-to-share-modified packet (*see figure 1d*) and wherein the second type of address packet is a proxy memory read packet (*see figure 1c*).

For claim 3, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to send a data packet corresponding to the coherency unit to the interface via the data network in response to receipt of the proxy read-to-share-modified packet (*see column 7, “Read Transactions”*).

For claim 15, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to send data corresponding to the coherency unit to the interface in

response to receipt of the proxy read-to-share-modified packet (*see column 7, "Read Transactions"*).

For claim 26, Liencres teaches an active device included in the node sending data corresponding to the coherency unit to the interface in response to receipt of the proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit (*see column 7, "Read Transactions"*).

For claim 4, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet (*see column 9, lines 22 – 31*).

For claim 16, Liencres teaches if the active device is the owner of the coherency unit, the active device is configured to lose its ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet (*see column 9, lines 22 – 31*).

For claim 27, Liencres teaches the active device losing the ownership responsibility for the coherency unit upon receipt of the proxy read-to-share-modified packet if the active device has the ownership responsibility for the coherency unit (*see column 9, lines 22 – 31*).

For claim 5, Liencres teaches if the active device has the ownership responsibility for the coherency unit, the active device is configured to transition an access right to the coherency unit upon sending the data packet on the data network (*see column 7, "Read Transactions"*).

For claims 6 & 22, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a directory in point-to-point mode (*see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode*).

For claim 28, Liencres teaches the address network conveying the first and second types of address packet from the interface to a directory in point-to-point mode (*see element 33 in figure 3a; having only 2 processors would, in effect, be a point-to-point mode*).

For claim 7, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to a plurality of devices included in the node in broadcast mode, wherein the plurality of devices include the system memory and the active device (*see column 4, lines 45 – 49*).

For claim 23, Liencres teaches the address network is configured to convey the first and second types of address packet from the interface to the plurality of devices in broadcast mode (*see column 4, lines 45 – 49*).

For claim 29, Liencres teaches the address network conveying the first and second types of address packet in broadcast mode (*see column 4, lines 45 – 49*).

For claims 8 & 21, Liencres teaches the data packet sent by the system memory includes an indication of the global access state of the coherency unit in the node (*see column 7, lines 48 – 52*).

For claim 9, Liencres teaches the coherency message requests a shared access right to the coherency unit (*see figure 1d*).

For claim 10, Liencres teaches the additional node is configured to send the coherency message in response to an additional active device included within the additional node sending an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the coherency unit, wherein the coherency unit is in a

shared global access state in the additional node, and wherein the node is a home node of the coherency unit (*see column 8, lines 63 – 68*).

For claim 30, Liencres teaches the additional node sending the coherency message in response to an additional active device included within the additional node sending an address packet on an additional address network included within the additional node, wherein the address packet requests write access to the coherency unit, wherein the coherency unit is in a shared global access state in the additional node, and wherein the node is a home node of the coherency unit (*see column 8, lines 63 – 68*).

For claims 11 & 31, Liencres teaches if the coherency unit is in the shared global access state in any of the plurality of nodes other than the home node, the coherency unit is in the shared global access state in the home node and no active device and no memory subsystem included in any of the plurality of nodes has the ownership responsibility for the coherency unit (*see figure 1a; see column 2, lines 15 – 24*).

For claim 12, Liencres teaches the interface is configured to send a copy of the coherency unit included in the data packet to the additional node (*see column 7, “Read Transactions”*).

For claim 20, Liencres teaches the data packet sent by the system memory includes a copy of the coherency unit (*see column 7, “Read Transactions”*).

For claim 32, Liencres teaches the interface sending a copy of the coherency unit included in the data packet to the additional node (*see column 7, “Read Transactions”*).

For claim 17, Liencres teaches the interface includes a global access state cache indicating global access states of a plurality of recently accessed coherency units in the node (*see element 31*).

For claim 18, Liencres teaches the interface is configured to check the global access state cache for the global access state of the coherency unit in the node, wherein if the global access state of the coherency unit is not included in the global access state cache, the interface is configured to request an indication of the global access state of the coherency unit from the system memory (*see column 9, lines 14 – 31*).

For claim 19, Liencres teaches the interface is configured to request the global access state of the coherency unit in the node from the system memory by sending the second type of address packet to the memory (*see column 9, lines 14 – 31*).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Examiner's Information

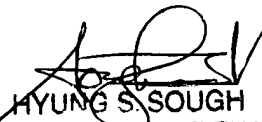
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Shawn Eland
12/13/2007



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12/20/07